CLAIMS

What is claimed is:

1. A method of designing an application specific integrated circuit (ASIC), comprising:

(a) performing static timing analysis on versions of an ASIC design multiple times before routing said ASIC design utilizing path delays that are estimated according to cardinality of fanout of nets of said ASIC design; and

(b) performing static timing analysis on versions of said ASIC design multiple times before routing said ASIC design utilizing path delays that are calculated from estimated routing distances within a current version of said ASIC design, wherein step (a) is performed more frequently than step (b).

2. The method of claim 1 further comprising:

determining from a Steiner tree analysis that said ASIC design does not satisfy a timing requirement.

3. The method of claim 1 further comprising:

flagging a circuit path of said ASIC design that does not satisfy a timing requirement.

4. The method of claim 3 further comprising:

repeating at least one ASIC design process to adapt said flagged circuit path to said timing requirement.

5. The method of claim 4 wherein said at least one ASIC design process is logical synthesis.

6. The method of claim 4 wherein said repeating at least one ASIC design process includes modifying a register transfer language description.

7. The method of claim 1 further comprising:

utilizing a static timing analysis estimated from a Steiner tree to modify a wire load model utilized to estimate timing delays associated with said cardinality of fanout of nets.

8. The method of claim 7 further comprising:

updating a wire load table.

9. The method of claim 8 wherein said wire load table comprises estimated capacitive loads of nets associated with a plurality of cardinal values of fanout.

10. The method of claim 1 further comprising:

routing said ASIC design; and

performing a timing analysis after performing said routing utilizing three-dimensional modeling of said ASIC design and lumped RC analysis.

11. A method of designing an application specific integrated circuit (ASIC), comprising:

(a) performing floor planning of an ASIC design;

(b) performing layout of said ASIC design;

(c) routing said ASIC design;

(d) performing static timing analysis on versions of said ASIC design multiple times during steps (a)-(b) utilizing path delays that are estimated according to cardinality of fanout of nets of said ASIC design; and

(e) performing static timing analysis on versions of said ASIC design multiple times during steps (a)-(b) utilizing path delays that are calculated from estimated routing distances within a current version of said ASIC design, wherein step (d) is performed more frequently than step (e).

12. The method of claim 11 further comprising:

determining from a Steiner tree analysis that said ASIC design does not satisfy a timing requirement.

13. The method of claim 11 further comprising:

flagging a circuit path of said ASIC design that does not satisfy a timing requirement.

14. The method of claim 13 further comprising:

repeating at least one ASIC design process to adapt said flagged circuit path to said timing requirement.

15. The method of claim 14 wherein said at least one ASIC design process is logical synthesis.

16. The method of claim 14 further comprising:

modifying a register transfer language description before repeating steps (a) and (b).

17. The method of claim 11 further comprising:

utilizing a static timing analysis estimated from a Steiner tree to modify a wire load model utilized to estimate timing delays associated with said cardinality of fanout of nets.

18. The method of claim 17 further comprising:

updating a wire load table.

19. The method of claim 18 wherein said wire load table comprises estimated capacitive loads of nets associated with a plurality of cardinal values of fanout.

20. The method of claim 11 further comprising:

performing a timing analysis on said routed ASIC design utilizing three-dimensional modeling of said ASIC design and lumped RC analysis.